



# CV

## Vasilis Gavrielatos

I am a Computer Science Ph.D. candidate with a focus on Computer Systems. My expected graduation date is summer 2021.

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## Interests and skills

### Distributed Systems

- Consensus, Replication
- Fault tolerance, Availability
- Key-Value-Stores, RDMA

### Computer Architecture

- Consistency, Persistency,
- Parallelism, Memory Systems

### Parallel Programming

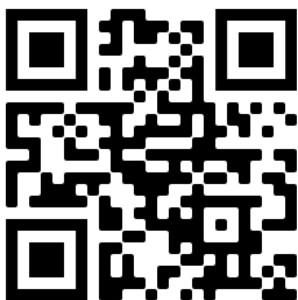
- Language-level memory models

### Software Engineering

- C, C++, Python, Linux

### Hardware Design

- VHDL, Verilog, SystemC
- ModelSim, Quartus



[vasiqavr1.github.io](https://vasiqavr1.github.io)

## Education

Since 2017  
University of  
Edinburgh

### Ph.D. in Computer Science

- Thesis: Enforcing Consistency in the Datacenter
- Advisor: Vijay Nagarajan; Secondary Advisor: Boris Grot
- Sponsored by ARM Centre of Excellence

2016-2017  
University of  
Edinburgh

### M.Sc. by research in Computer Science,

- Thesis: An RDMA-based skew-aware Key-Value Store
- Advisor: Vijay Nagarajan; Secondary Advisor: Boris Grot

2009-2015  
DUTH University

### B.Sc. & M.Sc. in Electrical & Computer Engineering

- Thesis: Heterogeneous links in VC-based Network-on-Chips
- Advisor: George Dimitrakopoulos

## Publications

EuroSys '21  
(to appear)

### Odyssey: The Impact of Modern Hardware on Strongly-Consistent Replication Protocols

- Designed Odyssey, a framework tailored towards replication protocol implementation for multi-threaded, RDMA-enabled, in-memory KVStores.
- Implemented and evaluated 10 protocols using Odyssey (including Paxos, ZAB & Hermes).
- Characterized the space of strongly-consistent replication protocols and demonstrated the interplay between modern hardware and protocols.

PaPoC '21  
(to appear)

### Abstracting consistency enforcement protocols with real-time orderings

- Proposed a mathematical model of consistency enforcement protocols.
- Created mapping from consistency models to said model, and a mapping from the model to protocol implementation techniques.

PPoPP '20  
Best paper  
nominee

### Kite: Efficient and Available Release Consistency for the Datacenter

- Designed Kite, the first highly-available, replicated Key-Value-Store that offers Release Consistency (and thus can be programmed similarly to C/C++11).
- Kite combines Eventual Store, ABD & Classic Paxos along with a novel fast/slow path mechanism to ensure both high-performance and availability.
- Demonstrated the efficacy of Kite by porting three lock-free data structures and showing that Kite outperforms the competition.

EuroSys '18

### Scale-out ccNUMA: Exploiting Skew with Strongly-Consistent Caching

- Designed a distributed, RDMA-enabled and multi-threaded Key-Value-Store that balances the load in the face of a skewed access pattern by symmetrically caching the most popular items in all nodes.
- Implemented two fully-distributed protocols to offer two flavours of consistency.

ASPLOS '20  
Micro Top Picks  
Honourable  
Mention

### Hermes: Fast and Reliable Data Replication with Linearizability

- Hermes is an RDMA-enabled, fault-tolerant replication protocol that offers Linearizability over a replicated Key-Value Store.
- Assisted in design space exploration, protocol design and the paper writing.
- Designed an RDMA-based version of ZAB to serve as a baseline.

ASPLOS '20

### Lazy Release Persistency

- A persistency model along with a microarchitectural technique that synergize with language-level memory models to ensure a consistent cut in the NVM after a crash.
- Assisted in design space exploration, technique design and paper writing.

ATC '21  
(submitted)

### Avocado: A Secure In-Memory Distributed Storage System

- Avocado is a secure replicated Key-Value Store that leverages Intel SGX, RDMA and the ABD protocol to achieve security, performance and consistency.
- Assisted in design space exploration, advised on enforcing consistency and RDMA.

## Work Experience

Since 2017

### Teaching at the University of Edinburgh,

- TA / Tutor / Marker & covering Lectures
- Classes: Computer Architecture, Introduction to Computer Systems
- Parallel Architectures

2016

### DSP engineer, Akya Limited, UK

- EDA tool design in C++